International Journal of Allied Practice, Research and Review
Website: www.ijaprr.com (ISSN 2350-1294)

Review of High Speed and Low Power ETSPC Based ÷ 2/3 Prescaler

Neetu Sharma and Mrs. Uma Nirmal
(M.tech.) VLSI, CET, Mody University of Science & Technology, Laxmangarh, Sikar, Rajasthan, India.
Assistant Professor, CET, Mody University of Science and Technology, Laxmangarh, Sikar, Rajasthan, India.

Abstract: Presently the investigation the power consumption is most essential factor for current VLSI circuits particularly for low power application. Frequencies dividers are also known as prescalers and are utilized as a part of numerous interchanges applications, for example, clock generation circuits, timing-recovery circuits, and frequency synthesizers. The design of fast and low-power prescaler is getting to be plainly noteworthy with the across the board utilization of cell phones and the request of longer battery life. This paper investigat's, distinctive 2/3 prescalers for low power applications. The paper speaks to a 2/3 dual modulus prescaler circuit, simulated at 180n CMOS process technology. The supply voltage of circuit is 1.0V.

Keywords: ETSPC, Prescaler, low voltage, low power, dual modulus prescaler

I. Introduction

An electronic counting circuit is known as prescaler and is utilized to decrease a high frequency electrical signal to a lower frequency by whole number division. It receipts the basic timer clock frequency and partitions it by some incentive before offering it to the clock, as indicated by which the prescaler registers are framed. The prescaler values that might be designed may be restricted to a few fixed values, or they might be any whole number an incentive from 1 to 2^P, where P is the number of prescaler bits. The rapid multi-GHz prescaler more often than not devours the biggest offer of energy in the frequency synthesizer in light of the fact that the prescaler is normally executed with advanced circuits with expansive power utilization at Gigahertz range. The highest operating frequency of clocked digital systems is controlled by the flip-flops. The right determination of flip-flop is especially vital which is done based on factors like high performance, low power, transistor count, clock load, design robustness, power delay, and power-area tradeoffs are by and large well-thoroughly

considered before picking a specific flip-flop design. Master-slave flip-flops are by and large used for low power frameworks though other flip-flop like pulse triggered flip-flops discovers their utilization in fast applications [1].

To satisfy the need of low voltage and high frequency circuit reasonable flip-flops must be chosen. Prescalers utilizing distinctive flip-flops are looked at as far as power, operating frequency, power-delay-product (PDP) and delay.

In present day wireless communication system, the MOS current mode logic circuit, which is of high power utilization, is usually used to accomplish the high operating frequency. The clock dynamic circuit with true single phase has switching power with low operating frequency [2][3]. Here ETSPC reasonable for higher operating frequency operations is discussed. Nonetheless extended true single phase clock causes high power utilization [4].

II. Dual Modulus Prescalers

The ETSPC based ÷2/3 unit Design-I in [5] is depicted in Figure 1. At the point when the modulus control signal MC is consistently high, the output of D Flip-Flop1 will be stopped to accomplish the ÷2 work. At the point when MC is set to low, it plays out the ÷3 work. In any case, both DFFs work regardless of whether DFF1 Doesn't takes an interest in the ÷2 work. The limitation of design-I circuit is that the power dissipation due to short circuit path is more since the load capacitance is large, the operating frequency is limited and the critical path is long.

Figure 2 shows the ETSPC based ÷2/3 unit Design-II [6]. The output of DFF1 will be clogged to accomplish the ÷2 work, when the modulus control signal MC is consistently high. At the point when MC is coherently low, it works as the ÷3. When MC=0 in ÷2 mode, short circuit path is absent in the second and third phase of D Flip-Flop1 and thus the power consumption is decreased. Design-II is superior to design-I since short circuit path is absent and consequently devour less power.

Figure 3 demonstrates the ETSPC based ÷2/3 prescaler design-III. In this short circuit path in two D Flip-Flops and transistor count is more. So the power consumption of design-III is high [7].

Figure 4 demonstrates the ETSPC based ÷2/3 prescaler design-IV. In addition to the speed advantage, Improved ETSPC Flip-flops are especially valuable for low voltage operations. Other than the two enhanced ETSPC FFs, just a single PMOS transistor is required. The divide control signal controls the PMOS Transistor which fills in as the switch. The AND gate in addition to its input inverter are accomplished by method for wired-AND logic utilizing no additional transistors by any stretch of the imagination. The design-IV scheme is significantly more modern than the measure of just including one pass transistor may recommend. Above all else, unlike to any past design, the Improved ETSPC (I ETSPC) FF configuration stays in place with no logic embedding. Both power and speed practices are not influenced, which demonstrates an performance edge over the logic embedded Flip-Flop design. The circuit rearrangements, again recommend the changes in both power and speed performance [8,9].

The operational guideline of design-IV is clarified as takes after. At the point when MC is "1", the P4 transistor is switched off as a switch ought to carry on. A single PMOS transistor, in any case, shows a little capacitive load to Flip-Flop1 than an inverter does in design. At the point when MC is "0", the output of Flip-Flop1, Q1b is tied with the output node of the first stage inverter of Flip-Flop2

through the P4 transistor. In an Improved ETSPC Flip-Flop design, the output of the first stage inverter can be considered complementary to the input [10].

In ÷ 2/3 prescaler Design-IV transistor count is less thus power dissipation and delay is less as compare to design-I and II [11].

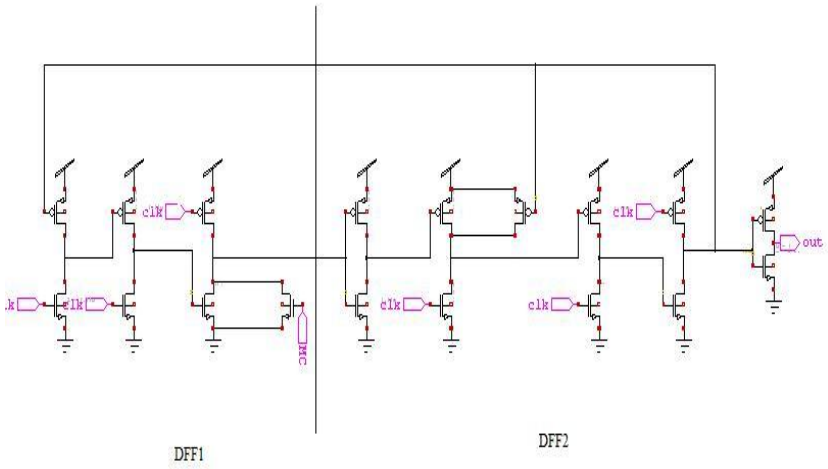

Fig.1 ETSPC based ÷ 2/3 Prescaler Design-I

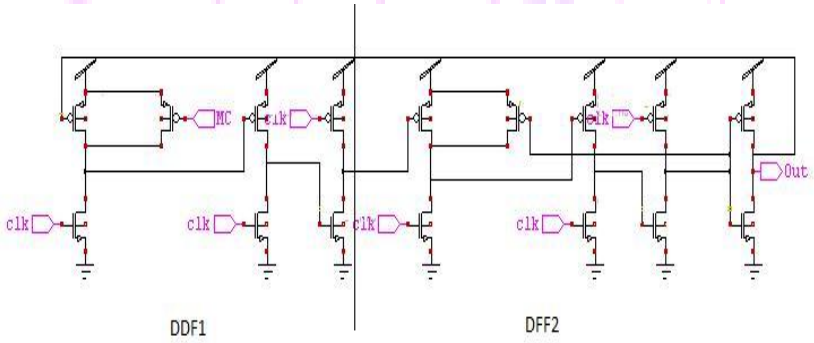

Fig.2 ETSPC based ÷ 2/3 Prescaler Design-II

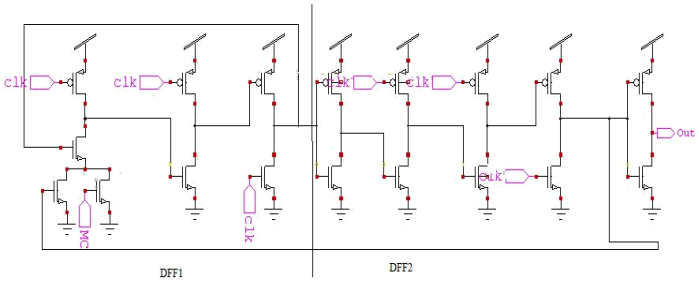

Fig.3 ETSPC based ÷ 2/3 Prescaler Design-III

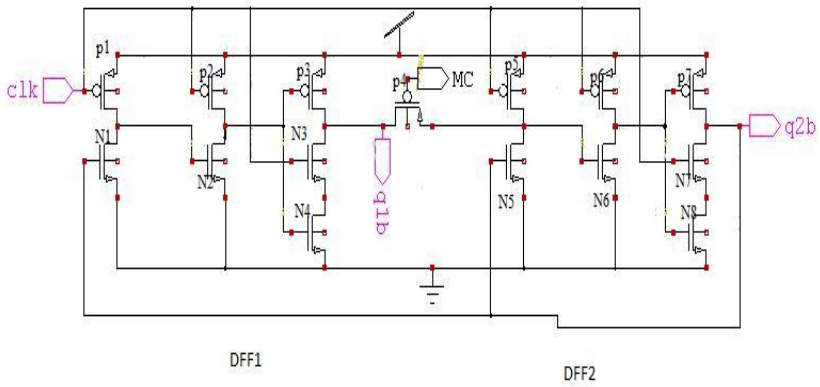

Fig.4 ETSPC based ÷ 2/3 Prescaler Design-IV

III. Comparison and Results

Figure 5,6 demonstrates the output waveform of ÷2 counter Design-I and ÷3 counter Design-I respectively. Design-I operating at 1.2V has the transistor count of 18 and is working at 180nm. The power consumed by ÷2 mode is 1.05 and ÷3 mode is 1.13. Figure 7,8 shows the output waveform of ÷2 counter design-II and ÷3 counter design-II respectively. Design-II operating at 1.2V has the transistor count of 16 and is working at 180nm. The power consumed by ÷2 mode is 1.02 and ÷3 mode is 1.11. Figure 9, 10 shows the output waveform of ÷2 counter design-IV and ÷3 counter Design-IV respectively. Design-IV operating at 1.0V has the transistor count of 15 and is working at 180nm. The power consumed by ÷2 mode is 0.095 and ÷3 mode is 0.092.

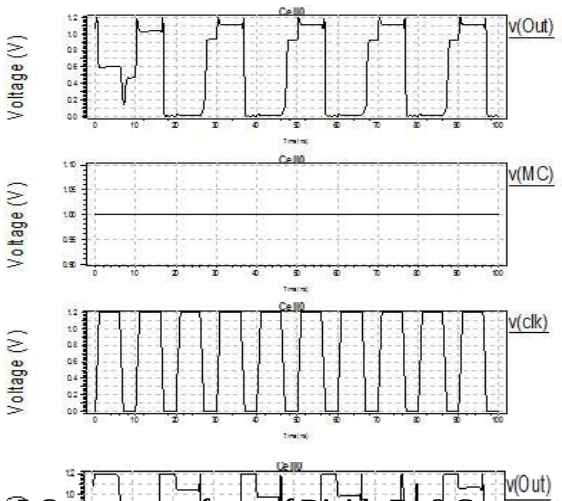

Fig.5 Output waveform of Divide By 2 Counter design-I

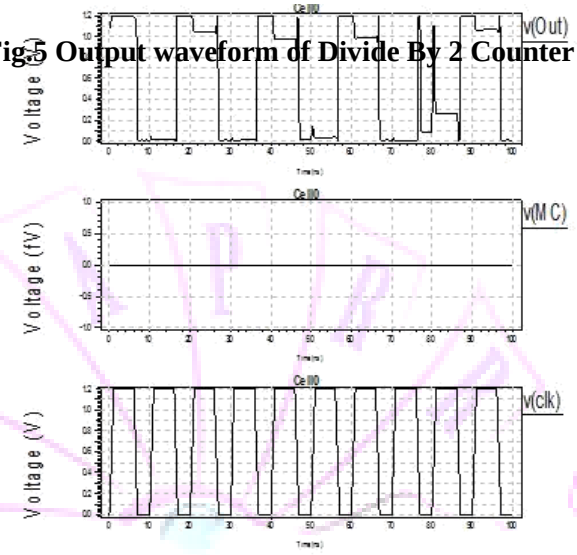

Fig.6 Output waveform of Divide By 3 Counter design-I

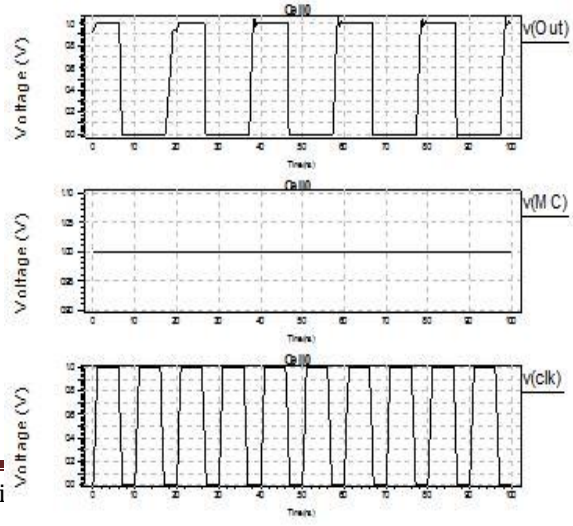

Fig.7 Output waveform of Divide By 2 Counter design-II

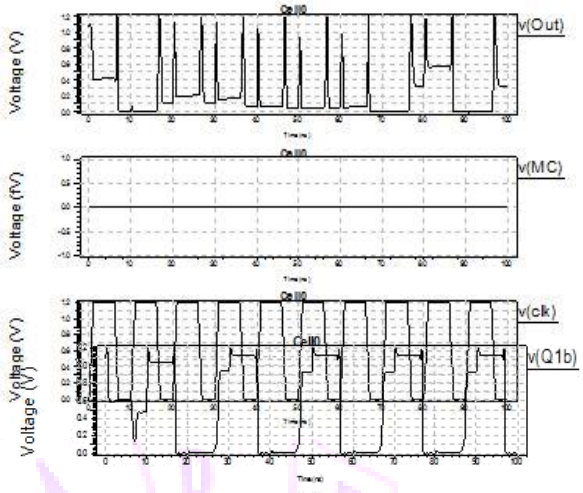

Fig.8 Output waveform of Divide By 3 Counter design-II

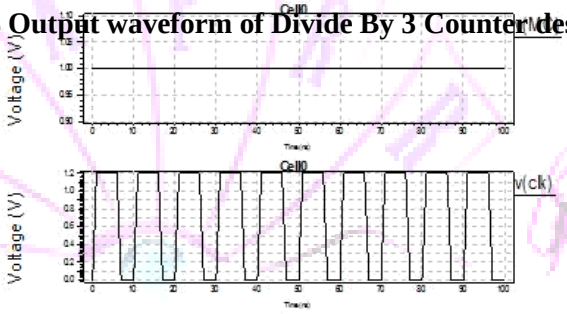

Fig.9 Output waveform of Divide By 2 Counter design-IV

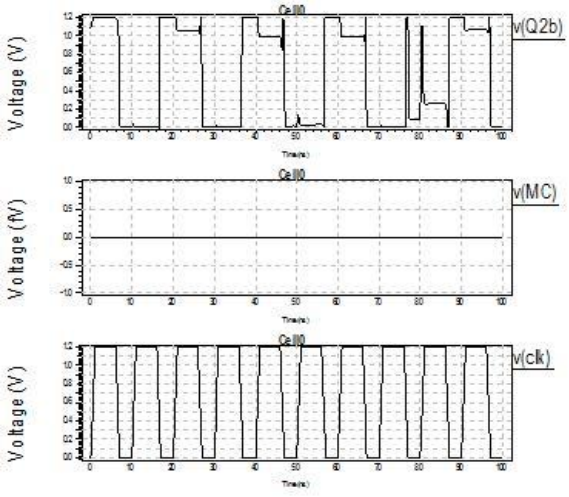

Fig.10 Output waveform of Divide By 3 Counter design-IV

Table I illustrates simulation performances of different dual modulus 2/3 prescalers and it is clearly visible that the results of Design-IV is much better than other prescaler. The Design-IV can operate properly up to 1.0V which is lower than the supply voltage of previous prescalers. Moreover, the transistor count in implementing the circuit as well as the power dissipation of Design-IV is much lower than the previous prescaler implemented in Design-I[5] and Design-II[6].

Table I Performance analysis of different dual modulus 2/3 prescalers

Design Parameters	**Design-I[5]**	**Design-II[6]**	**Design-IV[8]**
Transistor Count	18	16	15
Process(□ m)	0.18	0.18	0.18
Voltage(V)	1.2	1.2	1.0
Power(mW) ÷2 mode	1.05	1.02	0.095
Power(mW) ÷3 mode	1.13	1.11	0.092

IV. Conclusion & Future Scope

In this paper, I have implemented various ETSPC based ÷ 2/3 prescaler with better power and speed performance. ETSPC technique is used for circuits handling data with rates are double the clock rate. The dual modulus prescaler with ETSPC based ÷ 2/3 unit can be used in frequency divider. In Design-IV transistor count is less thus power dissipation and delay is less as compare to design-I and II.

V. Reference

[1] Song Jia, Ziyi Wang, Zijin Li, Yuan Wang,: "A Novel Low-Power and High-Speed Dual-Modulus Prescaler Based on Extended True Single-Phase clock logic"*978-1-4799-5341-7/16/$31.00 ©2016 IEEE*.

[2] Y. J. Ren, L Karlsso, and C. Svensson, " A True Single Phase Clock Dynamic CMOS Circuit Technique" IEEE Journal of solid-State Circuit, Vol.SC-22, No. 5, October 1987.

[3] Song Jia and Shilin Yan, "A Low-Power High-Speed 32/33 Prescaler Based on Novel Divide-by-4/5 Unit with Improved True Single-Phase Clock Logic", Circuits and Systems (ISCAS), Proceedings of 2015 IEEE International Symposium on, 2015 IEEE, May 2015.

[4] J. N. Soares, and W. A. M .Van Noije, "A 1.6-GHz Dual Modulus Prescaler Using the Extended True Single Phase Clock CMOS Circuit Technique (E-TSPC)", IEEE Journal of Solid-State Circuit, Vol. 34, No. 1, January 1999.

[5] S. Pellerano, and S.Levantino, "A 13.5 mW 5 GHz Frequency Synthesizer with Dynamic Logic Frequency Divider", *IEEE Journal of Solid-State Circuit,* Vol.39, No. 2,February 2004.

[6] X.P. Yu, M.A. Do, W.M. Lim, K.S. Yeo, J.-G. Ma,: "Design and Optimization of the Extended True Single-Phase Clock-Based Prescaler" *IEEE Transactions on Microwave Theory and Techniques*, Volume: 54, Issue: 11, Nov. 2006.

[7] Z. M. Deng and M. Niknejad, "The Speed-Power Trade-Off in the Design of CMOS True-Single-Phase-Clock Dividers", IEEE Journal of Solid-State Circuit, Vol. 45, No. 11, November 2010.

[8] Y.T.Hwang and J.F.Lin, "Low Voltage and Low power Divide-By-2/3 Counter Design Using Pass Transistor Logic Circuit Technique", *IEEE TransactionOn Very Large Scale Inegration(VLSI) Systems*, Vol. 20, No. 9, September 2012.

[9] Y. T. Hwang and J. F. Lin, "Low Voltage and Low Power Divide-By-2/3 Counter Design Using Pass Transistor Logic Circuit Technique",IEEE Transaction On Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 9, September 2012.

[10] X. P. Yu, M. A. Do, L. Jia, J. G. Ma, and K. S. Yeo,: "Design of a Low Power Wide-Band High Resolution Programmable Frequency Divider", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 13, NO. 9, SEPTEMBER 2005.

[11] Vamshi Krishna Manthena, Manh Anh Do, Chirn Chye Boon, and Kiat Seng Yeo:, "A Low-Power Single-Phase Clock Multiband Flexible Divider", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 2, FEBRUARY 2012.